

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

MICHIHISA MAEDA, ET AL.

Application No.:

Filed:

For: **Flip Chip Interconnection Using No-Clean
Flux**

Art Group:

Examiner:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Continuation Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Some or all of the references listed on the enclosed PTO/SB/08 were previously identified in the parent application (Application No. 09/820,547, filed March 28, 2001) and copies of the references were furnished at that time. Accordingly, per 37 CFR §1.98(d)(1) additional copies of those references are not submitted herewith.


The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Date: 1/21/04

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP


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US Department of Commerce Patent and Trademark Office Form PTO-1449 (Modified)			Atty. Docket No.: 42390P9978C		Application No.: Not Yet Assigned		
			Applicant: Maeda et al.				
			Filing Date: Concurrently Herewith				
US Patent Documents							
Examiner's Initials	Date	Document Number	Name	Class	Sub- Class	Filing Date	
	05/28/91	5,019,673	Juskey et al.			08/22/90	
	05/05/92	5,111,279	Pasch et al.			08/30/90	
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Examiner's Initials	Date	Document Number	Country	Class	Sub- Class	Translation	
	06/23/88	JP63151033	Japan				
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
Examiner				Date Considered			

Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw a line through the citation if not in conformance and not considered. Include a copy of this form with the next communication to the applicant

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US Patent Documents							
Examiner's Initials		Date	Document Number	Name	Class	Sub-Class	Filing Date
		01/06/98	5,704,116	Gamota et al.			
		04/17/01	6,217,671	Henderson et al.			
		05/02/00	6,057,168	Seyama et al.			
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		06/04/02	6,400,034	Kimura et al.			
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		09/01/88	63-004652	Japan			Y
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Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
		Pooya Tadayon, Sort Test Technology Development, Intel Corporation. "Thermal Challenges Diring Microprocessor Testing". Intel Technology Journal Q3, 2000. Pgs. 1-8.					
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Foreign Patent Documents							
Examiner's Initials		Date	Document Number	Country	Class	Sub- Class	Translation
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
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		Ravi Mahajan, Ken Brown & Vasu Atluri. "The Evolution of Microprocessor Packaging" Intel Technology Journal Q3, 2000. Pgs. 1-10.					
		Greig, W.J. "A Review of ThermoCompression Flip Chips Assembly", Electronic Packaging and Production, Pages 70-74, XP000776056.					
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